Course Code: 20EC4205 **R20**

SIDDHARTH INSTITUTE OF ENGINEEERING & TECHNOLOGY:: PUTTUR

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QUESTION BANK (DESCRIPTIVE)

Subject with Code: VERILOG HDL (20EC4205) **Course & Branch**: M.Tech-VLSI

Year & Sem: I-M.Tech & I-Sem **Regulation: R20**

UNIT - I
HARDWARE MODELING WITH THE VERILOG HDL

1.	a)	Explain structure design methodology with the verilog HDL.	[L2][CO1]	**[6M]**
	b)	Write verilog HDL structural model for a full sub tractor using NAND gates	[L3][CO2]	**[6M]**
2.	a)	Explain hardware modeling verilog primitives.	[L2][CO2]	**[6M]**
	b)	Illustrate behavioral description in verilog.	[L3][CO1]	**[6M]**
3. Explain the following descriptive styles of system hardware with the verilog HDL				
	a)	Structural description.	[L2][CO2]	**[6M]**
	b)	Behavioral description.	[L2][CO2]	**[6M]**
4.	a)	Explain structured design methodology.	[L2][CO2]	**[7M]**
	b)	Explain hierarchical descriptions of hardware	[L2][CO1]	**[5M]**
5.	a)	Discuss various descriptive styles available for hardware modeling using verilog HDL.	[L4][CO1]	**[8M]**
	b)	With neat flow graph, explain the TOP down design methodology relevant to hardware modeling using verilog HDL.	[L3][CO1]	[**4M]**
6.	a)	Explain the terms “Hardware Encapsulation” and “Hardware modeling” with suitable example using verilog HDL.	[L2][CO2]	**[6M]**
	b)	Describe hierarchical description of hardware modeling using verilog HDL.	[L3][CO1]	**[6M]**
7.	a)	Explain about Arrays of Instances in verilog with an example	[L2][CO3]	**7M]**
	b)	Write a brief notes on number representation in verilog.	[L3][CO2]	**[5M]**
8.	a)	Write a verilog program for 8x1 MUX using Structured Implicit model	[L3][CO3]	**[5M]**
	b)	Write a verilog program for Half adder using Structured Explicit model.	[L3][CO3]	**[7M]**
9.	a)	Explain any descriptive style of system hardware with the Verilog HDL with an example.	[L3][CO2]	**[6M]**
	b)	Write a brief note on language conventions in verilog.	[L3][CO3]	**[6M]**
10.	a)	Write a brief note on Hardware Modeling Verilog Primitives.	[L1][CO2]	**[6M]**
	b)	Write a program using TOP down design methodology in verilog.	[L2][CO1]	**[6M]**

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UNIT –II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL

1.		Explain in detail about verilog HDL data types with suitable examples.	[L2][CO1]	**[12M]**
2.	a)	What is user defined primitives? Explain combinational behavior of user defined primitives.	[L1][CO2]	**[7M]**
	b)	Explain conditional operator, operator precedence in VERILOG.	[L2][CO2]	**[5M]**
3.		Explain the following behavioral styles of system hardware with the verilog HDL		
	a)	Sequential Behavior.	[L2][CO1]	**[6M]**
	b)	Combinational Behavior.	[L3[CO1]	**[6M]**
4.		Discuss in detail about user defined behavioral system in verilog HDL.	[L2][CO2]	**[12M]**
5.	a)	Differentiate the combinational and sequential behavior of user-defined primitives for hardware modeling using verilog HDL.	[L2][CO2]	**[7M]**
	b)	Interpret the verilog models for transport delay with relevant examples.	[L2][CO1]	**[5M]**
6.	a)	Illustrate the initialization of sequential primitives with relevant examples.	[L3][CO2]	**[6M]**
	b)	Explain the terms “Inertial delay” and “Transport delay” relevant to verilog HDL models with suitable examples.	[L2][CO3]	**[6M]**
7.		Explain following concepts with example program.		
	a)	Verilog operators	[L2][CO2]	**[6M]**
	b)	Verilog variables.	[L2][CO1]	**[6M]**
8.		Explain following concepts with example.		
	a)	Verilog Expressions and Operands	[L2][CO2]	**[7M]**
	b)	Verilog Data Types	[L3][CO2]	**[5M]**
9.	a)	Write a brief notes on Path Delays and Simulation.	[L2][CO3]	**[5M]**
	b)	Explain the following i) Inertial Delay Effects ii) Pulse Rejection	[L2][CO2]	**[7M]**
10.	a)	Write a brief short notes on User Defined Primitives in verilog.	[L3][CO2]	**[6M]**
	b)	Explain Built-In Constructs for Delay in verilog.]	[L1][CO1]	**[6M]**

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UNIT –III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL

1.	a)	Explain behavioral statements in verilog HDL.	[L1][CO2]	**[6M]**
	b)	Discuss any two kinds of assignments in verilog HDL model with suitable examples.	[L2][CO3]	**[6M]**
2.	a)	Write short notes on non-blocking assignments and what are the sequences takes place at each positive edge of clock for the non-blocking assignments.	[L3][CO4]	**[7M]**
	b)	Explain behavioral models of finite state machine.	[L1][CO1]	**[5M]**
3.	a)	Write a short note on intra assignment delay.	[L2][CO4]	**[6M]**
	b)	Explain behavioral models of finite state machines.	[L3][CO2]	**[6M]**
4.	a)	How intra assignments delay control, event based timing control takes place in verilog HDL?	[L1][CO4]	**[7M]**
	b)	Write a verilog HDL program for Moore machine in behavioral models.	[L4][CO3]	**[5M]**
5.	a)	Explain how to summarize the various delays constructs in hardware modeling with the verilog HDL.	[L2][CO2]	**[6M]**
	b)	Explain the concept of 'constructs for activity flow control'.Give the behavioral description in verilog HDL.	[L1][CO3]	**[6M]**
6.	a)	Explain the behavioral descriptions for simulation of simultaneous procedural assignment used in verilog HDL with suitable example.	[L2][CO1]	**[8M]**
	b)	Interpret the Indeterminate Assignments and Ambiguity in verilog.	[L3][CO4]	**[4M]**
7.	a)	How the timing checks can be given in system tasks in verilog.	[L4][CO2]	**[6M]**
	b)	Draw the ASM chart for the dice game and write a program in behavioral models verilog HDL	[L1][CO3]	**[6M]**
8.	a)	Write short notes on Simultaneous Procedural Assignments.	[L4][CO4]	**[7M]**
	b)	What is the differences between an initial behavior and an always behavior	[L1][CO1]	**[5M]**
9.	a)	Give a Summary of Delay Constructs in Verilog.	[L3][CO2]	**[6M]**
	b)	Write a short note on Variable Scope Revisited in verilog.	[L2][CO4]	**[6M]**
10	Explain the following.			
	a)	Procedural Continuous Assignments	[L2][CO2]	**[6M]**
	b)	Procedural Assignment	[L2][CO4]	**[6M]**

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UNIT –IV

SYNTHSIS OF COMBINATIONAL LOGIC

1.	a)	Draw the block diagram for HDL based synthesis explain each block	[L1][CO3]	**[6M]**
	b)	Explain the tree state buffers.	[L3][CO2]	**[6M]**
2.	a)	Draw the block diagram for test bench for post synthesis design verifications.	[L4][CO4]	**[6M]**
	b)	Discuss about behavioral synthesis.	[L2][CO1]	**[6M]**
3.	a)	Explain the block in the logical synthesis.	[L1][CO3]	**[6M]**
	b)	Discuss about RTL synthesis.	[L2][CO4]	**[6M]**
4.	a)	Function of 'F' that is to be decomposed in terms of new nodes x & y the original form of **F=ABC+ABD+$\overline{ACD}$ + $\overline{BCD}$**	[L4][CO2]	**[8M]**
	b)	Discuss the synthesis of priority structures with one example.	[L3][CO1]	**[4M]**
5.	Explain the following.			
	a)	Simulation efficiency	[L2][CO2]	**[7M]**
	b)	Procedural continuous assignments	[L1][CO3]	**[6M]**
6.	a)	Write, verify and synth size a 16 bit adder sub tractor.	[L3][CO4]	**[8M]**
	b)	Explain the synthesis of user defined function.	[L2][CO3]	**[4M]**
7.	a)	Write a program for synthesis of user defined tasks?	[L4][CO4]	**[6M]**
	b)	Write a program for synthesis of case and conditional.	[L1][CO1]	**[6M]**
8.	a)	What is synthesis of the disable statements write any one program for it.	[L2][CO4]	**[6M]**
	b)	Explain the non-blocking assignments of synthesis.	[L3][CO2]	**[6M]**
9.	a)	Draw the flow chart for synthesis of loops explain each block?	[L1][CO4]	**[7M]**
	b)	Write program for synthesis of multi cycle operations.	[L4][CO2]	**[5M]**
10.	a)	Explain the types of timing controls in synthesis.	[L1][CO1]	**[7M]**
	b)	Discuss the fork &join blocks.	[L2][CO4]	**[5M]**

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UNIT –V

SWITCH-LEVEL MODELS IN VERILOG

1	a)	Discuss why switch level is useful?	[L3][CO1]	**[7M]**
	b)	Give the MOS transistor technology?	[L1][CO2]	**[5M]**
2	a)	Write and verify a switch level al a three input static CMOS NOR gate?	[L3][CO3]	**[6M]**
	b)	Explain the truth table for switch level MOSFET transistor module?	[L2][CO1]	**[6M]**
3	a)	Write and verify the switch level for JK flip flop having preset and clear input?	[L3][CO3]	**[7M]**
	b)	Draw the circuit diagram of CMOS and explain it?	[L2][CO4]	**[5M]**
4	a)	Design & verify a switch level model at the four channel MOS transistor	[L1][CO2]	**[5M]**
	b)	Discuss about alternative loads and pull gates?	[L2][CO1]	**[7M]**
5	a)	Explain the CMOS transmission gates with diagram?	[L3][CO2]	**[4M]**
	b)	Write a test bench and simulate the behavior at the circuit in fig. 	[L4][CO4]	**[8M]**
6	a)	Explain the types of signal strengths?	[L1][CO3]	**[6M]**
	b)	Draw & explain the circuit diagram of CMOS switch with a program.	[L2][CO2]	**[6M]**
7	a)	Discuss about Ambiguous signals?	[L3][CO1]	**[6M]**
	b)	Write a program for NMOS Three input NOR gate?	[L2][CO3]	**[6M]**
8	Explain the following.			
	a)	Strength reduction by primitives	[L2][CO1]	**[7M]**
	b)	Transistor switch & bi-directional switch	[L3][CO3]	**[5M]**
9	a)	Design the circuit diagram for CMOS NOR gate?	[L2][CO2]	**[6M]**
	b)	Implement NAND, AND, OR gates using MOS switch test it with a suitable test bench?	[L3][CO1]	**[6M]**
10	Write a program for NMOS inverter with pull up loads?		[L2][CO2]	**[12M]**

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